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Criterion 3: Research, Innovations and Extension

Key Indicator 3.3- Research Publication and Awards

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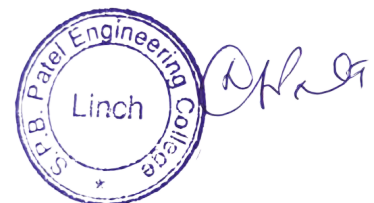


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Response:

1. Cover page,
2. The first page of the chosen- publication
3. Web link of Journal/book





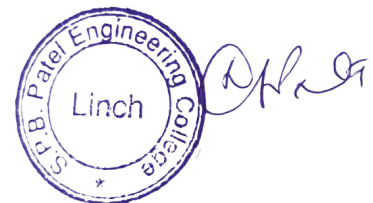
[1] Title Name: Analysis of a New Symmetric Multilevel Inverter Topology with Reduced Component Count

~ Prof. Nirav Joshi

Calendar Year of publication: 2020

1. Cover page of Journal/book:

The screenshot shows the IEEE Xplore search interface. At the top, there are navigation links for IEEE.org, IEEE Xplore, IEEE SA, IEEE Spectrum, and More Sites. The main header includes the IEEE Xplore logo, a search bar, and options for 'Browse', 'My Settings', 'Help', and 'Institutional Sign In'. A dropdown menu under 'Help' shows 'Contact Us' and 'Resources and Help'. Below the header, there's a search bar with 'Search within results' and buttons for 'Export', 'Set Search Alerts', and 'Search History'. The search results section shows 'Showing 1 of 1 result for International Conference on Emerging Trends in Information Technology and Engineering (ic-ETITE) x Analysis of a New Symmetric Multilevel Inverter Topology with Reduced Component Count x'. There are filters for 'Conferences (1)', 'Show' (All Results, Open Access Only), 'Year' (Range, Single Year), and 'Sort By' (Relevance). The search results list the paper title, authors (Nirav Ratilal Joshi, Amit Vilas Sant), conference name (2020 International Conference on Emerging Trends in Information Technology and Engineering (ic-ETITE)), year (2020), publisher (IEEE), and cited by (Papers (2)). There are also promotional banners for 'Need Full-Text' and 'Get Published in the IEEE Open Journal of Systems Engineering'.





2. First Page of Publication:

2020 International Conference on Emerging Trends in Information Technology and Engineering (ic-ETITE)

Analysis of a New Symmetric Multilevel Inverter Topology with Reduced Component Count

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Abstract— Medium voltage drives (MVDs) are increasingly used in industrial applications. Like any *ac* drive, MVDs employ inverter to modulate the power being supplied to the *ac* motor so as to match the speed–torque characteristic of the motor with that of the load. The only distinguishing feature is that MVDs operate at the voltage levels of 2.2, 3.3, 4.16, or 6.6 kV. Presently, the solid state technology is such that the power semiconductor switches that operate at medium voltage are not easily available. Multilevel inverter (MLI) emerges as the ideal choice for MVDs as it can overcome this issue with the series connection of switches that is inherent to its power structure. However, MLI topologies often suffer from high switch/diode count. This paper proposes a new symmetrical MLI topology with reduced component count. A comparison of the proposed MLI topology with the earlier reported topologies is presented in this work for the different levels of output voltages. Furthermore, the operation of the proposed 7–level MLI topology supplying a three phase induction motor is analyzed for steady state.

Keywords— Induction motor drive, medium voltage drive, multilevel inverter, reduced switch multilevel inverter topology

I. INTRODUCTION

Globally, the industrial drives are the major consumers of electric energy. In USA, industrial drives consume about 60% to 65% of the generated electric power [1]. The industrial drives fed from medium voltage (MV) grids at 2.2, 3.3, 4.16 or 6.6 kV, [2], are termed as medium voltage drives (MVD). MVDs covers a wide power range, from 0.4 MW to almost 40 MW at the MV level of 2.3–13.8 kV. The high-power MVDs find wide applications in petrochemical and cement industries, water pumping stations, traction systems, steel rolling mills, etc [3]. Reference [4] has reported the installation of 1–4MW MVDs that operate at 3.3–6.6 kV.

Inverters are integral part of any *ac* drives and act as an interface to modulate power being delivered to the induction motors. With MVDs being deployed for the speed control of induction motors, they are a sub-set of *ac* drives. With the present state of solid state technology, power semiconductor switches operating at MV levels are not easily available. However, multi-level inverters (MLIs) involve series connection of multiple power semiconductor switches and are ideal power modulators for MVDs. References [5–8] have reported MLI based MVDs. Moreover, with the reduction in voltage total harmonic distortion (THD) at the output of MLI as compared to the 2–level inverter, the motor efficiency is further improved.

MLIs are *dc-ac* power converters that comprise of an array of power semiconductor switches to provide stepped *ac* voltages of the desired levels. As compared to the traditional 2–level inverter, MLI offers the benefits of lower distortion

in output voltages, reduced *dv/dt* and voltage stress for power semiconductor switches, lower filtering requirements, ease of operation at higher voltage and power levels and reduced electromagnetic interference [9–12]. The three basic topologies of MLI are (i) Diode clamped or neutral point clamped (NPC) MLI, (ii) Flying capacitor (FC) or capacitor clamped MLI and (iii) Cascaded H-Bridge (CHB) MLI. Along with some emerging topologies of MLI, José Rodríguez et al have surveyed the basic topologies and presented a detailed analysis [2]. These topologies suffer from increase in switch or diode or capacitor count. The increased switch count necessitates increased gate drivers, protection units, which further adds to the system complexity and cost. Hence, there is a strong need for reduced switch MLI topology [13].

References [14–16] have presented different reduced switch MLI topologies. These inverter topologies are mainly classified as (i) symmetric reduced switch MLI, and (ii) asymmetric reduced switch MLI. In symmetric reduced switch MLI, values of all the *dc* sources are equal [13, 17–18]. Conversely, in asymmetric reduced switch MLI, the values of *dc* sources are unequal. Symmetric configuration of the MLI topology offers the benefits of good modularity and comparatively simple modulation and control. In [19], a modular MLI topology has been proposed wherein an H–bridge along with a bidirectional switch is used to produce 5–level single phase output waveform. Peng et al, in [20], have proposed a generalized MLI topology, wherein basic cells are employed to obtain multilevel stepped voltages. However, for 7–level unidirectional output voltage, the reported topology requires thirty switches.

This paper proposes a new symmetrical MLI topology with reduced switch count for MVD application. The paper proposes *n*–level multilevel inverter topology that has number of switches $(n + 7)/2$. Compared to the generalized MLI topology, for a single phase 7–level configuration, the proposed topology requires seven switches and six diodes, in which three switches generate zero, V_{dc} , $2V_{dc}$, and $3V_{dc}$ voltage levels. Additional four switches are required to generate bidirectional supply. However, the voltage balancing, explored in [20], is not included in this work. The operation of the proposed topology is compared with the three basic topologies and the topology reported in [20]. Moreover, the operation of proposed MLI topology with 7–level voltage output is analyzed for an MVD driving a 3–phase induction motor.

II. MEDIUM VOLTAGE DRIVES

MVDs are operated at medium voltage, 2.2, 3.3, 4.16 or 6.6 kV, to improve the motor efficiency. As the industrial drives are the major consumer of the total generated electric

3. Web link of journal/ book:

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